CLAIMS

What is claimed is:

1. A library core for embedded passive components, comprising:

an insulating core layer having an upper surface and a lower surface opposed to the upper surface, and formed with a plurality of openings penetrating therethrough;

a plurality of areas provided for embedded passive components and defined by the openings of the core layer filled with passive component materials therein;

electrically conductive layers formed over the upper and lower surfaces of the core layer respectively.

2. The library core for embedded passive components of claim 1, wherein the electrically conductive layer is patterned to form a plurality of conductive traces for electrically interconnecting the areas provided for embedded passive components and defined by the openings.
3. The library core for embedded passive components of claim 2, wherein the passive components are resistors.
4. The library core for embedded passive components of claim 2, wherein the passive components are capacitors.
5. The library core for embedded passive components of claim 3, wherein the conductive traces are partly used as electrodes of the resistors.
6. The library core for embedded passive components of claim 4, wherein the conductive traces are partly used as parallel sheets of the capacitors.
7. The library core for embedded passive components of claim 1, wherein the core layer is formed with a plurality of conductive vias for electrically interconnecting the electrically conductive layers on the upper and lower surfaces of the core layer.
8. The library core for embedded passive components of claim 2, wherein the library

core with the patterned conductive traces is fabricated in a semiconductor packaging substrate or printed circuit board for enhancing performances of electrical characteristics.

9. The library core for embedded passive components of claim 2, wherein the library core with the patterned conductive traces is formed with an insulating layer over the conductive traces on the core layer and formed at least one circuit layer on the insulating layer so as to form a multi-layer circuit board.

10. The library core for embedded passive components of claim 9, wherein the multi-layer circuit board is fabricated in a flip-chip semiconductor packaging substrate.

11. The library core for embedded passive components of claim 9, wherein the multi-layer circuit board is fabricated in a wire-bonding semiconductor packaging substrate.

12. A method for forming an electronic device on a library core for embedded passive components, comprising the steps of:

providing an insulating core layer having an upper surface and a lower surface opposed to the upper surface, wherein the core layer is formed with a plurality of openings penetrating therethrough, allowing the openings to be filled with passive component materials, and electrically conductive layers are formed over the upper and lower surfaces of the core layer respectively;

patterning the electrically conductive layers respective on the upper and lower surfaces of the core layer to form a plurality of conductive traces for electrically interconnecting the passive component materials contained in the openings of the core layer, to thereby form the library core with the embedded passive components; and

mounting and electrically connecting the library core with the embedded

passive components to the electronic device.

13. The method of claim 12, wherein the passive components are resistors.

14. The method of claim 12, wherein the passive components are capacitors.

15. The method of claim 13, wherein the conductive traces are partly used as electrodes of the resistors.

16. The method of claim 14, wherein the conductive traces are partly used as parallel sheets of the capacitors.

17. The method of claim 12, wherein the core layer is formed with a plurality of conductive vias for electrically interconnecting the conductive traces on the upper and lower surfaces of the core layer.

18. The method of claim 12, wherein the electronic device is selected from the group consisting of a semiconductor packaging substrate and printed circuit board.